Remarks:

Reconsideration of the application is requested.

Claims 1 and 6-20 are now in the application. Claims 1, 6 and 7 have been amended. Claims 2-5 have been cancelled. Claim 20 has been added.

In item 3 on page 2 of the above-mentioned Office action, claims 1-19 have been rejected as being anticipated by Tomita, Dukes et al. or Kirihata et al. under 35 U.S.C. § 102(b). In item 6 on page 2 of the above-mentioned Office action, claims 1-19 have been rejected as being anticipated by Tuttle, Akram, Cook et al. or White et al. under 35 U.S.C. § 102(e).

The rejections have been noted and claim 1 has been amended in an effort to even more clearly define the invention of the instant application. More specifically, the features of claims 2 and 3 have been added to claim 1. Claim 20 has been added.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claims 1 and 20 calls for, respectively, inter alia:

> said energy source having at least one solar cell for generating an operating current for said semiconductor chip by optical radiation that is fed in contactlessly.

Tomita discloses a semiconductor integrated circuit having a light emitting device. The light emitting device is used to monitor the state of the circuit by observing the light pattern of the device. In contrast to the invention of the instant application, the circuit includes a light emitting device rather than an energy source for providing an electrical energy supply generating an operating current for a semiconductor chip by optical radiation that is fed in contactlessly. This applies similarly to Dukes et al., which describe an electronic circuit including a built-in self-test circuit having a visual indicator which is a light emitting diode.

Kirihata et al. describe an integrated circuit chip incorporating a self-test system. As described in column 5, lines 17 to 45, an operation power is applied to the chip being placed in a chuck, which supplies power to all the power pins (lines 38 to 39). In contrast to the invention of the instant application, the Kirihata at al. reference does not disclose any energy source on a chip having a solar cell for generating an operating current for a semiconductor chip according to the invention.

Cook et al. relate to devices for testing semiconductor wafers during manufacturing and, more specifically, to testing

devices which do not contact the device under test. The device includes a circuit including a power generator for generating power when exposed to light. However, Cook at al. do not disclose a beneficial arrangement of solar cells for generating an operating current for the semiconductor chip according to the invention of the instant application. Cook at al. rather show pure electrical schematics including a light powered generator, a radio frequency generator and a light source to power the device under test.

The Tuttle reference describes a testing system using RF communication. In contrast to the invention of the instant application, power transfer is established via radio communication rather than optical radiation. Accordingly, Tuttle does not disclose a chip arrangement comprising solar cells according to the invention of the instant application.

Akram discloses a burn-in testing system for evaluating a circuit under test including a burn-in board having a plurality of receptacles. The circuit under test is configured to be connected to a power supply to power the circuit under test during burn-in testing (see abstract; column 5, lines 10 to 12; and Fig. 2). There, no solar cell arrangement according to the invention of the instant application is shown.

White et al. describe a method and apparatus for wireless testing of integrated circuits via electromagnetic response signals or radio-frequency signals. However, White et al. do not disclose a solar cell arrangement on a semiconductor chip according to the invention of the instant application.

Clearly, none of the cited references shows "said energy source having at least one solar cell for generating an operating current for said semiconductor chip by optical radiation fed in contactlessly", as recited in claims 1 and 20 of the instant application.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1 or claim 20. Claims 1 and 20 are, therefore, believed to be patentable over the art and since all of the dependent claims are ultimately dependent on claim 1, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1 and 6-20 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

Please charge any fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

For Applicants

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Marked-Up Version of the Amended Claims:

Claim 1(amended). A test configuration, comprising:

a [support material] semiconductor wafer;

a plurality of semiconductor [chip] chips disposed on said [support material] semiconductor wafer, each of said plurality of semiconductor [chip] chips having a self-test unit generating test information for functionally checking said semiconductor chip; and

an energy source for providing an electrical energy supply from energy [that is] fed in contactlessly, said energy source disposed on said [support material] semiconductor wafer and connected to said semiconductor chip for providing the electrical energy supply to said semiconductor chip, said energy source having at least one solar cell for generating an operating current for said semiconductor chip by optical radiation fed in contactlessly;

said semiconductor wafer having a scribe line for separating said plurality of semiconductor chips from one another, and said solar cell being disposed in said scribe line.

Claim 6(amended). The test configuration according to claim [2] 1, wherein said solar cell is disposed on a surface of said [support material] semiconductor wafer which is remote from said semiconductor chip, said [support material] semiconductor wafer having an electrically conductive plated-through hole formed therein disposed between said solar cell and said semiconductor chip, at a boundary between said plated-through hole and said [support material] semiconductor wafer, said [support material] semiconductor wafer has a pn junction disposed along said plated-through hole for preventing a current flow between said plated-through hole and a remainder of said [support material] semiconductor wafer.

Claim 7(amended). The test configuration according to claim [4] 1, including a radiation-absorbing layer disposed between said solar cell and said semiconductor chip.